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Realization of Peres Gate as Universal Structure using Quantum Dot Cellular Automata

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ABSTRACT

The problems pertaining to scaling which the conventional technologies were facing was successfully addressed with the novel technology known as Quantum-dot Cellular Automata (QCA). The principle spin and anti-spin has been already employed for representation of the binary logic states. The QCA has exploited the concept of spin and evolved a new computational paradigm where the position of electrons decides about the logic states. Power dissipation is the main limitation of all the nanoelectronics design techniques including the QCA. Researchers have proposed the various mechanisms to limit this problem. Among them, reversible computing is considered as the reliable solution to lower the power dissipation. In reversible computing, the primitive building blocks are the reversible logic gates. This paper explores the Peres gate as the universal structure as all the basic logic gates have been derived from this gate only. All the proposed logic gate designs were simulated and their credibility was successfully verified with the QCA Designer tool.

1. Introduction

The scaling is used to increase the number of transistors in a given area of an IC, reducing the delay time, operation at high frequency and low power consumption. But this scaling faces serious challenges too. Over decades the CMOS has successfully achieved these goals but it cannot sustain forever due to the fundamental physical limits. Thus there is a desperate need to find an alternative to conventional CMOS technology. Various alternative nano scale technologies have been proposed but QCA emerged as the favorite candidate to replace the CMOS technology. QCA is a promising nanotechnology that provides the unique properties that arise when the dimensions are reduced to nano scale [1, 2].

QCA paradigm offers a new model of computation where the binary information is stored as the position of electrons in the QCA cell rather than the voltage levels as the conventional technologies were utilizing especially the CMOS. In logic circuit design the heat dissipation is a serious issue which needs to be addressed. Research is going on to have a methodology that will result in the energy efficient systems. One possible solution is to use the concept of reversible computing. In 1961 Landauer [3] succeeded to establish a relation between the information loss and the energy dissipation. According to Landauer's principle any logic circuit which loses the information will result in energy dissipation of the order of K_BTln2, (where and T the absolute temperature and K_B is the Boltzmann's constant). Furthermore Bennett in 1973 showed that if the reversible logic gates will be employed for logic circuit design it will result in the efficient circuits with ideally zero power dissipation. Thus Bennett's theorem stressed the use of reversible computation technological necessity that future technology will require to reduce power loss [4]. Thus reversible gates preserve the information rather than to lose it as in conventional logic gates. Conventional logic gates are not energy efficient because they are not reversible. A circuit can achieve the reversibility if

1. The number inputs vector is equal to output vector.
2. The mapping is one-one between the input and output.

An inverter is reversible circuit as it satisfies the both the conditions of reversibility. While as an AND gate is not a reversible one because the output "0" occurs at the three different input combinations (e.g. 00, 01, 10) hence it is not possible to recover an input vector from an output. This information loss leads to the energy dissipation. Some of the well-known reversible gates are Feynmann gate [5], Toffoli gate [6], Peres [7] gate, Fredkin gate [8] etc. In addition several other reversible gates have also been reported in open literature [9-14]. The potential of the reversible computing can be exploited to design the low power nano computing devices and future technologies.

2. Experimental Methods

2.1 QCA Architecture

The basic computational block of the QCA technology is the QCA cell that stores the logic states as charge in traps, positioned at the four corners of the square shaped geometry. The charge traps are known as the quantum dots. Only two mobile electrons are permitted to reside inside the cell. The mobile electrons acquire the diagonal positions due to columbic force of repulsion thereby resulting the two possible polarizations that correspond to 0 and 1. Fig. 1 shows the two QCA cell polarizations.

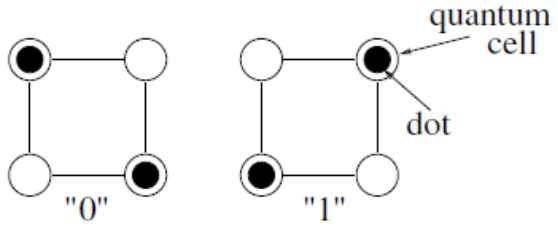

Fig. 1 QCA cell polarizations and representations of binary 0 and binary

By arranging the QCA cells in some predefined fashion the different devices like majority logic gate, inverter etc., can be obtained as shown in Fig. 2.

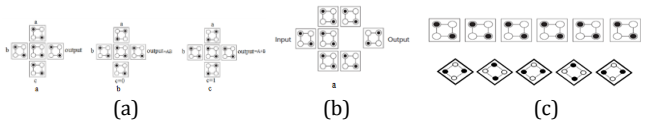

Fig. 2 (a) Majority logic gate (b) QCA Inverter and (c) QCA Wire

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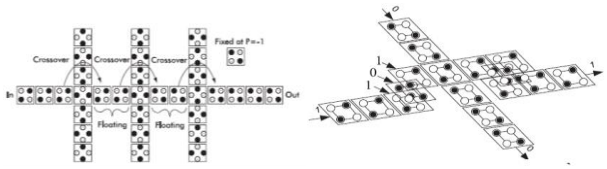
The majority logic gate is considered as the backbone of QCA technology as most of the logic circuits are designed around the majority gate shown in Fig. 2 (a). It consists of three inputs labeled as A, B, C and single output. The centre cell is referred as driver cell and it switches to major polarization depending on the polarity of the inputs. The logic equation of the majority gate can be realized as:

$$M(A,B,C) = AB + BC + AC \quad (1)$$

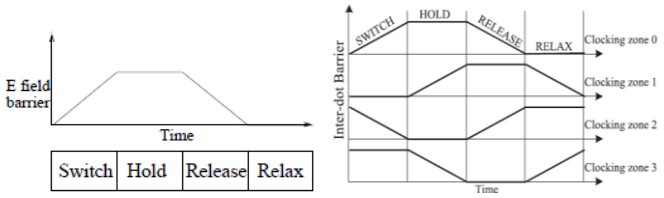
By fixing one of the input to +1 or -1, the AND & OR functions can be obtained. The inverter is also an important component of QCA which can be implemented either with seven cells, four cells or two cells as shown in fig. QCA technology has two types of wires 90 °C wire which allows the signal to propagate through it without changing its original state. While as the 45 °C wire allows the designer to obtain the uncomplimented as well as complemented form of an input signal thereby eliminating the use of explicit inverters. One of the unique features of the QCA is to allow the wire crossing in a single plain without interference, this type of crossing is known as coplanar crossing. QCA also provides flexibility to have wire crossing in different plains by utilizing the multi-layer crossovers. Fig. 3 shows the two QCA wire types.



(a) (b)

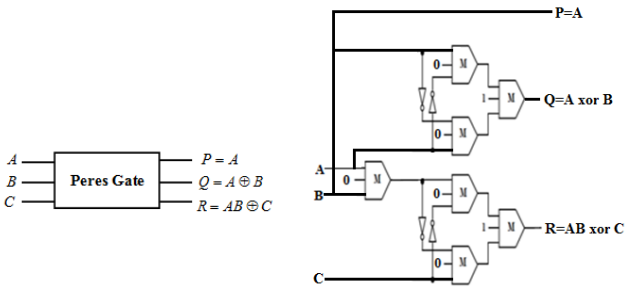
Fig. 3 (a) Coplanar wire crossing and (b) Multi layer wire crossing

Every logic circuit needs a driving source for signal flow. The QCA clock is used to provide the synchronization, control information flow and supply the power to run the circuit. The QCA works on four phase clocking mechanism. A QCA circuit works under the influence of four clock zones and each clock zone consists of four phases, which are Switch, Hold, Release and Relax. During the switch phase, the barriers are raised and the QCA cells start to attain a particular polarization and settles down to one of the possible ground polarization states. During the hold phase, barriers are maintained high enough to freeze the electron tunneling and hence cell states remain unchanged. The release phase facilitates the cell to attain the unpolarized state by changing the barriers from high to low. After the release phase the barriers remain unaltered (i.e. lower state) and hence the cell continues to remains in the same unpolarized state. Fig. 4 illustrates the QCA clock scheme.



(a) (b)

Fig. 4 (a) 4 phase clocking and (b) Switching in a binary wire



(a) (b)

Fig. 5 (a) Block Diagram of Peres gate and (b) MV representation of Peres gate

3. Results and Discussion

3.1 Peres Gate

Peres gate is universal logic gate and all the basic logic functions can be implemented using the Peres gate only. It is a 3 x 3 gate, means it has three inputs and three outputs. The input vector is defined as *I (A, B, C)* and the output vector is represented as *O (P, Q, R)*. The relationship between the inputs and the outputs are defined as: $P = A$, $Q = A \oplus B$ and $R = AB \oplus C$ respectively. The schematics and the MV layout of the Peres gate is shown in (Figs. 5a and b).

The truth table of the 3 x 3 Peres gate is given in Table 1.

Table 1 Truth table of Peres gate

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

From the Table 1 it is clear that the output P is equal to the input A the output Q is equal to XOR of the inputs A & B. The third output(R) is inverted when the first two inputs are equal to 1. For any boolean function *f (x1, x2, x3,....xn)* there is a circuit consisting of Peres gates which takes *(x1, x2, x3,....xn)* as inputs and provides the *(y1, y2, y3,....yn)* as outputs.

The QCA implementation and the simulation results of Peres gate are shown in (Figs. 6 & 7).

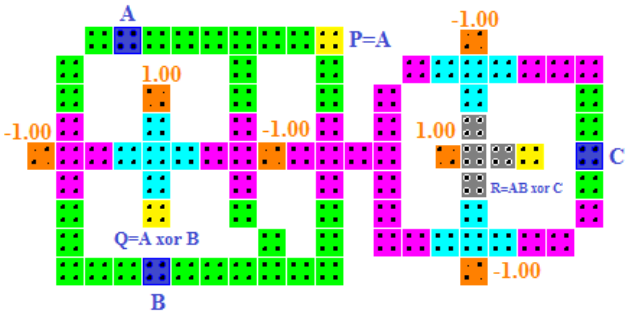


Fig. 6 QCA implementation of Peres gate

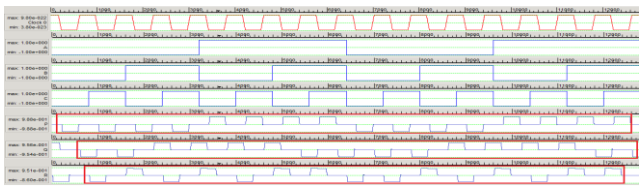


Fig. 7 Simulation Result of Peres gate

Table 2 Comparison of various Peres gates

Circuit	No. of Layers	Cell count	Cell Area (μm²)	Total Area (μm²)	Latency (in clock cycles)
Peres gate [15]	1	99	0.0320	0.0819	1
Peres gate [16]	4	273	0.0884	0.3745	2
Proposed Peres gate	1	87	0.0281	0.0583	1

Table 3 Basic gate functions obtained using Peres gate

S. No	Circuit	Peres Gate Function
01	NOT GATE	*Peres* (*A*,1,1)
02	AND GATE	*Peres* (*A*,*B*,0)
03	OR GATE	*Peres* ($\bar{A}$,$\bar{B}$,1)
04	NAND GATE	*Peres* (*A*,*B*,1)
05	NOR GATE	*Peres* ($\bar{A}$,$\bar{B}$,0)
06	EX-OR GATE	*Peres* (*A*,1,*C*)
07	EX-NOR GATE	*Peres* (*A*,1,$\bar{C}$)

The Peres gate is designed with seven majority gates. Five majority gate provides the AND function and the two perform the OR operation. The outputs P and Q are garbage outputs and are not required in the computations. The comparison of the various QCA based Peres gate and the proposed one is given in the Table 2.

Table 2 clearly indicates that the proposed QCA based Peres gate is efficient in terms of cell count, cell area, total area, latency and complexity as compared to the previous designs available in the open literature. The Peres gate can be realized as the universal gate as all the basic gate functions can be implemented by Peres gate alone. By selecting the proper inputs the basic logic gates can be designed by using the parameters mentioned in Table 3.

The QCA implementation of the various logic gates designed with the Peres gate are shown in the (Figs. 8a-g).

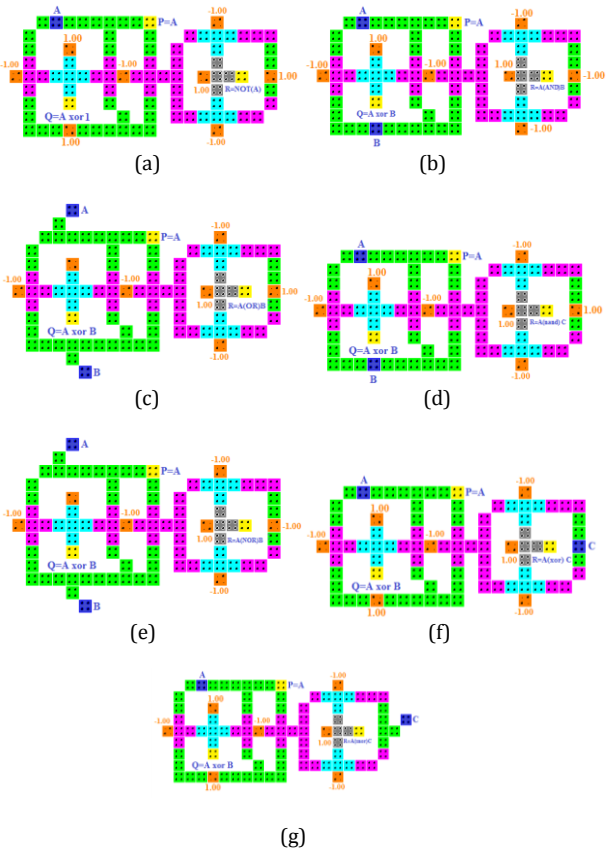
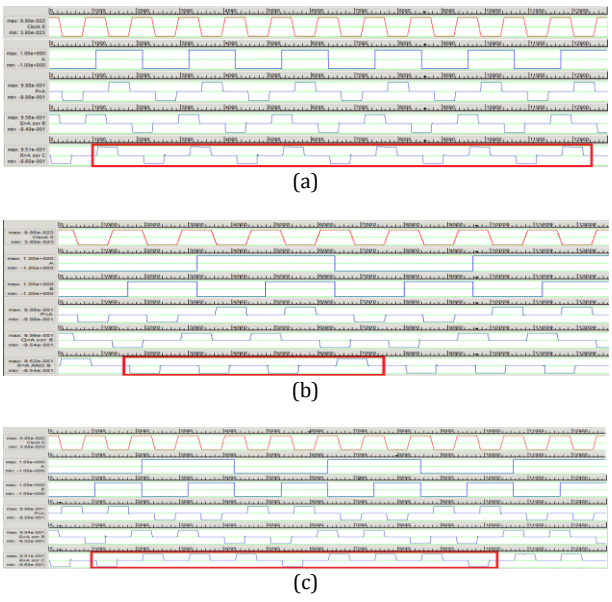


Fig. 8 QCA implementation of Peres gate based (a) NOT gate (b) AND gate (c) OR gate (d) NAND gate (e) NOR gate (f) EX-OR gate and (g) EX-NOR gate

The simulation results of QCA based logic gates using Peres gate are shown in (Fig. 9a-g).



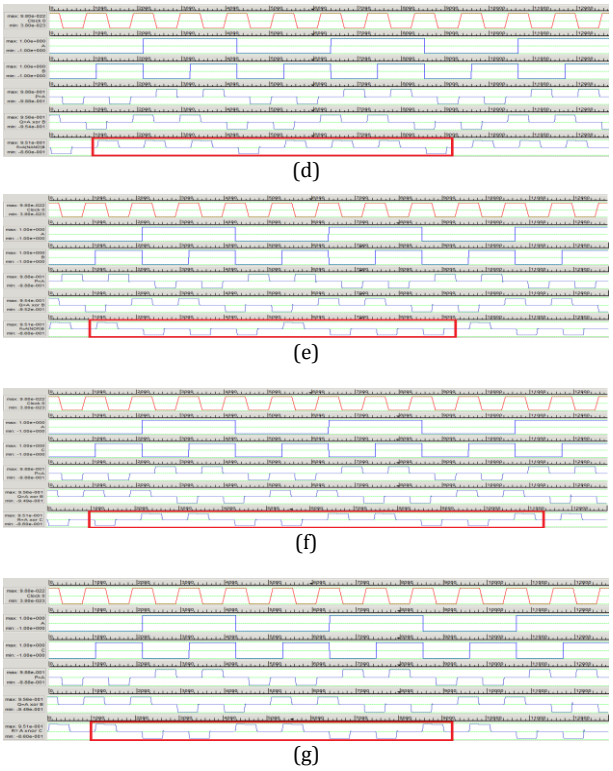


Fig. 9 Simulation results of Peres gate based (a) NOT gate (b) AND gate (c) OR gate (d) NAND gate (e) NOR gate (f) EX-OR gate and (g) EX-NOR gate

The reduction in the cell count of the proposed Peres gate is illustrated in Fig. 10.

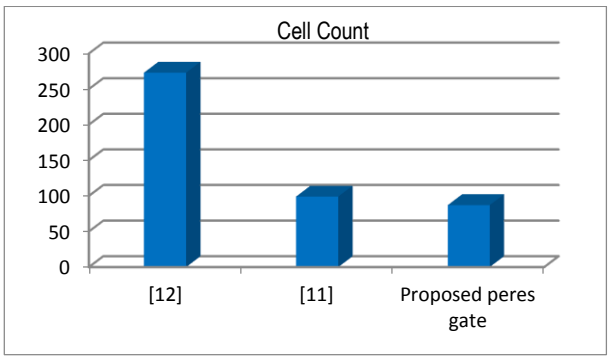


Fig. 10 Comparative figures of cell count of Peres gate

The simulations were carried out using the QCA Designer tool using the bistable approximation under the following specified parameters.

- Cell Size = 18 nm
- Cell Spacing = 2 nm
- Number of Samples = 12800
- Radius of Effect = 65.000000 nm
- Convergence Tolerance = 0.001000
- Relative Permittivity = 12.900000
- Clock High = 9.800000e - 022
- Clock Amplitude Factor = 2.000000
- Layer Separation = 11.500000.

4. Conclusion

In this paper, Peres gate was implemented using quantum dot cellular automata and was realized as the universal gate. The proposed QCA implementation of Peres gate can be extended to design the classical logic gates. The proposed QCA structures are efficient in term of cell count, cell area, latency and complexity can be used in the design of combinational and sequential circuits that would prove to be beneficial in respect of power saving, reduction of garbage outputs and less amount of delay. Besides, being reversible all the designs will enjoy low energy dissipation, simple testability and increased fault detection features.

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